

### **REMARKS**

Claims 1-5, 7, and 9-22 are pending in this application. By this Response, claims 1, 3, 5 and 7 are amended, claims 6 and 8 are canceled, and claims 9-22 are added. Support for the amendments to claims 1, 3, 5 and 7 and newly added claims 9-22 may be found at least in Figure 3 and pages 7-9 of the present specification. No new matter has been added by any of the amendments or new claims presented in this Response. Reconsideration of the claims in view of the above amendments and the following remarks is respectfully requested.

#### **I. Telephone Interview**

Applicants thank Examiner Moazzami for the courtesies extended to Applicants' representative during the February 22, 2006 telephone interview. During the telephone interview, the above amendments and distinctions of the claimed invention over the cited art were discussed. Examiner Moazzami agreed that the above amendments to the claims appear to overcome the rejections set forth in the previous Office Action. However, Examiner Moazzami requested that Applicants provide an explanation in Applicants' written Response of the difference between the mapping of the L1 cache in the Edirisooriya et al. reference (U.S. Patent Publication No. 2004/0111563) to the system memory and the local store alias portion recited in the amended claims. The explanation is provided hereafter. The substance of the telephone interview is summarized in the following remarks.

#### **II. Rejection under 35 U.S.C. § 103(a)**

The Office Action rejects claims 1-8 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Applicants' Allegedly Admitted Prior Art (referred to hereafter as AAPA) in view of Bauman (U.S. Patent No. 6,587,931). This rejection is respectfully traversed.

Claim 1, which is representative of the other rejected independent claims 3, 5 and 7 with regard to similarly recited subject matter, reads as follows:

1. A non-homogeneous multiprocessor system, comprising:  
a first processor coupled to a first local store;  
a first cache associated with said first processor;  
one of a second processor or other device non-homogeneous with said first processor;  
multiprocessor bus means connected to said first cache of said first processor and to said one of a second processor or other device non-homogeneous with said first processor for providing cache coherent communications via said bus means; and  
a system memory having a coherent memory space, the system memory being shared by the first processor and the one of a second processor or other device non-homogeneous with said first processor, wherein the coherent memory space in system memory includes a local store alias portion that maps a local store address space into a real address space of the system memory, and wherein the one of a second processor or other device non-homogeneous with said first processor accesses the first local store of the first processor using the local store alias portion of the coherent memory space in the system memory.

(emphasis added)

Neither the allegedly admitted prior art (AAPA) nor Bauman, either alone or in combination, teaches or suggests a system memory having a coherent memory space that includes a local store alias portion that maps a local store address space into a real address space of the system memory. Moreover, neither reference, whether taken alone or in combination, teaches or suggests that a second processor or other device that is non-homogeneous with a first processor accesses a first local store of the first processor using the local store alias portion of the coherent memory space in the system memory.

The AAPA in the background of the present application teaches that caches associated with processors in a homogeneous processor system may be accessed and tables associated with the caches may be made consistent. The AAPA further teaches that homogenous multiprocessor systems may perform atomic updates of a memory location and a mechanism for performing atomic updates using a DMA unit is generally known. The AAPA also teaches that heterogeneous multiprocessor systems are generally

known in the art. However, nowhere in the AAPA is there any teaching or suggestion to provide a system memory having a coherent memory space that includes a local store alias portion that maps a local store address space of a local store associated with a heterogeneous processor into a real address space of a system memory.

Bauman teaches a directory based cache coherency system that supports multiple instruction processors and input/output caches. Bauman is cited by the Office Action as allegedly teaching multiple heterogeneous instruction processors which allows the shared memory to be modified on other than strictly cache line boundaries. While Bauman teaches that a system may be comprised of multiple heterogeneous instruction processors, nowhere in Bauman is there any teaching or suggestion to provide a system memory having a coherent memory space that includes a local store alias portion that maps a local store address space of a local store associated with a heterogeneous processor into a real address space of a system memory.

Thus, since neither reference teaches or suggests such a coherent memory space that includes a local store alias portion, as recited in claim 1, any alleged combination of the AAPA and Bauman, even if such a combination were possible and one of ordinary skill in the art were somehow motivated to make such a combination, *arguendo*, would not result in the features of claim 1 being taught or suggested. Moreover, since neither reference, either alone or in combination, teaches or suggests such a coherent memory space including a local store alias portion, neither reference, either alone or in combination, teaches or suggests that a second processor or other device non-homogeneous with a first processor accesses the first local store of the first processor using the local store alias portion of the coherent memory space in the system memory.

During the February 22, 2006 telephone interview, Examiner Moazzami agreed that neither the AAPA nor Bauman teach or suggest these features of claim 1 or the similar features found in amended independent claims 3, 5 and 7. Thus, it is Applicants' understanding that Examiner Moazzami is in agreement that the rejection of claims 1-5 and 7 under 35 U.S.C. § 103(a) based on the AAPA and Bauman should be withdrawn. Accordingly, for the reasons set forth above, Applicants respectfully request withdrawal of the rejection of claims 1-5 and 7 under 35 U.S.C. § 103(a) based on the AAPA and Bauman.

### III. Rejection under 35 U.S.C. § 103(a)

The Office Action rejects claims 1-8 under 35 U.S.C. § 102(e) as being allegedly anticipated by Edirisooriya (U.S. Patent Application Publication No. 2004/0111563). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). Applicants respectfully submit that Edirisooriya does not identically show every element of the invention as recited in independent claims 1, 3, 5 and 7 arranged as they are in the claims.

Edirisooriya is directed to a method and apparatus for providing cache coherency between heterogeneous agents and limiting data transfers among symmetric processors. As shown in Figure 1, the system of Edirisooriya may include a plurality of processors 140 and 160 which may heterogeneous with one another (see paragraph 13 where processors 140 and 160 are referred to as "agents"). The heterogeneousness in Edirisooriya is with regard to whether the processor supports ownership or not in the writeback capability of the caches 142, 162 of the processors. That is, the processors 140 and 160 may include MESI or MOESI level one caches 142, 162. The mechanism of Edirisooriya is directed to resolving a situation in which one processor uses a MOESI protocol cache that supports ownership and another processor uses a MESI protocol cache that does not support ownership.

With regard to claim 1, Edirisooriya does not teach or even suggest to provide a system memory having a coherent memory space that includes a local store alias portion that maps a local store address space of a local store associated with a heterogeneous processor into a real address space of a system memory. Moreover, Edirisooriya does not teach or even suggest that a second processor or other device non-homogeneous with a

first processor accesses the first local store of the first processor using the local store alias portion of the coherent memory space in the system memory. To the contrary, Edirisooriya makes not mention at all regarding any mapping of a local store to system memory, let alone using such a mapping so that one processor or non-homogenous device is able to access the local store of a different processor. To the contrary, all memory accesses in Edirisooriya are between a single processor and its cache or the system memory. There is no teaching or suggestion in Edirisooriya for one processor to access a local store of another processor, let alone by using a coherent memory space in system memory that includes a local store alias portion that maps the local store address space to a real address space of the system memory.

During the February 22, 2006 telephone interview, Examiner Moazzami stated that the local caches 142, 162 of the processors 140, 162 in Edirisooriya may be considered to be local stores and that the processors 140, 162 are heterogeneous. Moreover, Moazzami alleged that while the Edirisooriya reference does not provide any teaching to the affect, there would need to be some mapping between the caches 142, 162 and the system memory. Examiner Moazzami requested that Applicants provide argument to distinguish over such mapping.

While there may be a mapping between individual caches 142, 162 and the system memory for writeback purposes, there is no teaching or suggestion in Edirisooriya that one processor, e.g., processor 140, may use this mapping between cache 162 and the system memory 110 to access the cache 162 associated with processor 160. To the contrary, the mapping, if there is any, would be exclusively used between that particular cache 162 and the system memory 110 to perform writeback operations. The processor 140 is not taught as having any access to such a mapping. Moreover, there is no teaching that the processor 140 could access such a mapping for purposes of accessing the cache 162 of another processor 160. Thus, even if the Examiner is correct that there is a mapping between the L1 caches 142, 162 of the processors 140 and 160, the Edirisooriya reference still does not teach each and every feature of claim 1 or similar features found in the other rejected independent claims 3, 5 and 7.

In view of the above, Applicants respectfully submit that Edirisooriya does not teach each and every feature of independent claims 1, 3, 5 and 7 as is required under 35

U.S.C. § 102(e). At least by virtue of their dependency on claims 1 and 3, respectively, Applicants respectfully submit that Edirisooriya does not teach each and every feature of dependent claims 2 and 4. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-5 and 7 under 35 U.S.C. § 102(e).

#### **IV. Newly Added Claims**

Claims 9-22 are added to recite additional features of the present invention that are not taught or suggested by the AAPA, Bauman, or Edirisooriya. Specifically, claim 9 is added to recite that the second processor or other device non-homogenous with the first processor is a second processor and that the second processor is one of a control processor or a data plane processor. Similar features are added in new claims 13 and 17.

Claims 10, 14 and 18 are added to recite that the first processor/second heterogeneous device accesses a portion of data in a second local store associated with a second processor/first heterogeneous device using the local store alias portion and that the portion of data accessed in the second local store is cached in a first cache associated with the first processor/second heterogeneous device. As discussed above, none of the cited references teach or suggest using a local store alias portion to access a local store of a processor or non-homogeneous device and furthermore, do not teach or suggest to cache data accessed in this manner in a cache associated with the processor/non-homogeneous device accessing the local store.

Claims 11, 15 and 19 recite similar features with different processors/non-homogeneous devices performing the accessing of local stores. These claims are likewise not taught or suggested by the cited references.

Claims 12, 16 and 20 are added to recite that transfers between the local store and the system memory are performed using the local store alias portion. None of the cited references teach or suggest to use the same local store alias portion to provide access to a local store by a processor not directly associated with the local store and to also perform data transfers between the local store and system memory, as recited in these claims.

Independent claims 21 and 22 recite a method and computer program product for accessing a local store associated with a processor, the processor being one of a plurality

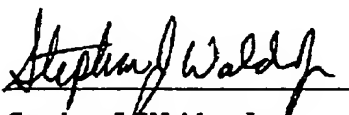
of heterogeneous processors. The method and computer program product include an operation and computer readable program, respectively, for mapping a local store address space of a local store associated with a second processor of a plurality of heterogeneous processors into a real address space of a system memory using a local store alias portion of a coherent memory space of the system memory. The method and computer program product further include an operation and computer readable program, respectively, for accessing, by a first processor, the local store of the second processor using the local store alias portion of the coherent memory space in the system memory. These features are similar to features added by amendment to independent claims 1, 3, 5 and 7 and thus, are distinguished over the cited references for similar reasons as set forth above with regard to claims 1, 3, 5 and 7.

V. **Conclusion**

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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